

CLAIMS

I claim:

1. A system for use with a power supply, comprising:

two double-layer capacitors, the two double-layer capacitors operatively coupled to output terminals of the power supply, wherein each double-layer capacitor comprises a capacitance of greater than or equal to 1 Farad;

a voltage balancing circuit; the voltage balancing circuit operatively coupled to the two double-layer capacitors to balance a power supply voltage applied to the two capacitors; and

a current control device, the current control device including a feedback portion, the current control device coupled to output terminals of the power supply, wherein the current control device controls current flowing through the two double-layer capacitors according to a signal provided by the feedback portion.

2. The system of claim 1, wherein the feedback portion is operatively coupled to the voltage balancing device so as to provide a positive feedback signal to the voltage balancing device.

3. The system of claim 1, wherein the feedback portion is operatively coupled to the voltage balancing device so as to provide a negative feedback signal to the voltage balancing device.

4. A circuit for coupling an energy storage device to an output of a first power supply, the circuit comprising:

a current-sensing resistor;

a switch comprising a pair of outputs coupled in series with the energy storage device and with the current-sensing resistor, and an input receiving a switching signal, the switch assuming a conducting state when the switching signal is at a first level, the switch assuming a non-conducting state when the switching signal is at a second level;

30 a differential high-gain device comprising an output coupled to the input of the
31 switch, a first input biased by a control voltage, and a second input receiving feedback
32 voltage generated by a charging current flowing through the current-sensing resistor;

33 wherein:

34 the output of the differential high-gain device drives the input of the switch with the
35 switching signal at the first level when the control voltage exceeds the feedback voltage
36 by an input offset voltage of the differential high-gain device, and the differential high-
37 gain device drives the input of the switch with the switching signal at the second level
38 when the feedback voltage exceeds the control voltage by the input offset voltage; and

39 the current-sensing resistor, the switch, and the energy storage device are coupled
40 across the output of the first power supply.

41
42 5. A circuit according to claim 4, further comprising a mechanism generating the control
43 voltage as a function of a voltage appearing at the output of the first power supply,
44 wherein the control voltage increases monotonically with the voltage appearing at the
45 output of the first power supply.

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47 6. A circuit according to claim 4, wherein the differential high-gain device comprises an
48 operational amplifier.

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50 7. A circuit according to claim 4, wherein the differential high-gain device comprises
51 CMOS circuitry.

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53 8. A circuit according to claim 4, wherein the differential high-gain device comprises a
54 low-offset device.

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56 9. A circuit according to claim 4, wherein the differential high-gain device comprises a
57 comparator.

58
59 10. A circuit according to claim 4, wherein the switch comprises a discrete transistor.

- 61 11. A circuit according to claim 4, wherein the switch comprises a discrete power
62 transistor.
- 63
- 64 12. A circuit according to claim 4, wherein the switch comprises a MOSFET.
- 65
- 66 13. A circuit according to claim 4, wherein the switch comprises an analog
67 semiconductor switch.
- 68
- 69 14. A circuit according to claim 4, further comprising a current-limiting resistor coupled
70 between the output of the differential high-gain device and the input of the switch.
- 71
- 72 15. A circuit according to claim 4, further comprising a first resistor and a second resistor
73 coupled in series to form a voltage divider, the voltage divider being coupled across the
74 output of the first power supply, the voltage divider generating the control voltage at a
75 junction of the first and second resistors.
- 76
- 77 16. A circuit according to claim 15, wherein the differential high-gain device comprises a
78 low-offset device.
- 79
- 80 17. A circuit according to claim 16, wherein the first and second resistors are precision,
81 temperature-stable resistors.
- 82
- 83 18. A circuit according to claim 17, wherein the differential high-gain device comprises
84 CMOS circuitry.
- 85
- 86 19. A circuit according to claim 4 further comprising the energy storage device.
- 87
- 88 20. A circuit according to claim 19, wherein the energy storage device comprises a
89 capacitor.
- 90

21. A circuit according to claim 19, wherein the energy storage device comprises a double layer capacitor.

22. A circuit according to claim 19, wherein the energy storage device comprises at least two capacitors and a voltage balancer.

23. A circuit according to claim 19, wherein the energy storage device comprises a secondary battery cell.

24. A circuit according to any one of claims 4, further comprising a second power supply, the second power supply comprising input connections coupled across the output of the first power supply to receive power from the first power supply at a first nominal voltage, and an output providing electrical power at a second nominal voltage to a load.

25. A circuit according to claim 24, wherein the second power supply comprises a regulator.

26. A circuit according to claim 24, wherein the second power supply comprises a DC-to-DC power converter.

27. A circuit according to claim 24, wherein the second nominal voltage exceeds the first nominal voltage by about 7 volts.

28. A circuit according to claim 24, wherein the first nominal voltage is about 5 volts, and the second nominal voltage is about 12 volts.

29. A circuit for coupling an energy storage device to an output of a first power supply, the circuit comprising:

- a switch comprising a pair of outputs coupled in series with the energy storage device to form a series combination, the series combination being coupled across the output of the first power supply, and an input receiving a switching signal, the switch assuming a

conducting state when the switching signal is at a first level, the switch assuming a non-conducting state when the switching signal is at a second level;

a connection receiving a voltage reference signal; and

a differential high-gain device comprising an output coupled to the input of the switch, a first input biased by a control voltage, and a second input receiving the voltage reference signal;

wherein:

the control voltage is monotonically related to a voltage appearing at the output of the first power supply so that the differential high-gain device drives the input of the switch with the switching signal at the first level when the control voltage exceeds the voltage reference signal by an input offset voltage of the differential high-gain device, and the differential high-gain device drives the input of the switch with the switching signal at the second level when the voltage reference signal exceeds the control voltage signal by the input offset voltage.

30. A circuit according to claim 29, further comprising a voltage reference source generating the voltage reference signal.

31. A circuit according to claim 30, further comprising a first resistor and a second resistor coupled in series with the first resistor to form a voltage divider, the voltage divider being coupled across the output of the first power supply, the voltage divider generating the control voltage at a junction of the first and second resistors.

32. A circuit according to claim 31, wherein the differential high-gain device comprises a low-offset device.

33. A circuit according to claim 31, wherein the first and second resistors are precision, temperature-stable resistors.

34. A circuit according to claim 33, wherein the differential high-gain device comprises CMOS circuitry.

153
154 35. A circuit according to claim 31, further comprising the energy storage device.
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156 36. A circuit according to claim 35, wherein the energy storage device comprises a
157 capacitor.
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159 37. A circuit according to claim 35, wherein the energy storage device comprises a
160 double layer capacitor.
161
162 38. A circuit according to claim 35, wherein the energy storage device comprises at least
163 two capacitors and a voltage balancer.
164
165 39. A circuit according to claim 35, wherein the energy storage device comprises a
166 rechargeable battery cell.
167
168 40. A circuit according to claim 31, wherein the differential high-gain device comprises
169 an operational amplifier.
170
171 41. A circuit according to claim 31, wherein the differential high-gain device comprises
172 CMOS circuitry.
173
174 42. A circuit according to claim 31, wherein the differential high-gain device comprises a
175 comparator.
176
177 43. A circuit according to claim 31, wherein the switch comprises a discrete transistor.
178
179 44. A circuit according to claim 31, wherein the switch comprises a discrete power
180 transistor.
181
182 45. A circuit according to claim 31, wherein the switch comprises a MOSFET.
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184 46. A circuit according to claim 31, wherein the switch comprises an analog
185 semiconductor switch.

186
187 47. A circuit for coupling an energy storage device to an output of a first power supply,
188 the circuit comprising:

189 a switch comprising a pair of outputs coupled in series with the energy storage device
190 to form a first series combination, the first series combination being coupled across the
191 output of the first power supply, and an input receiving a switching signal, the switch
192 assuming a conducting state when the switching signal is at a first level, the switch
193 assuming a non-conducting state when the switching signal is at a second level;

194 a connection receiving a voltage reference signal;

195 a first resistor and a second resistor coupled in series to form a second series
196 combination comprising a junction of the first and second resistors, the second series
197 combination being coupled across the output of the first power supply;

198 a differential high-gain device comprising an output coupled to the input of the
199 switch, a non-inverting input coupled to the junction of the first and second resistors, and
200 an inverting input receiving the voltage reference signal; and

201 a positive feedback resistor coupled between the output of the differential high-gain
202 device and the non-inverting input of the differential high-gain device.

203
204 48. A circuit according to claim 47, further comprising a voltage reference source
205 generating the voltage reference signal.

206
207 49. A circuit according to claim 48, wherein the differential high-gain device comprises a
208 low-offset device.

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210 50. A circuit according to claim 49, wherein the first, second, and positive feedback
211 resistors are precision, temperature-stable resistors.

212
213 51. A circuit according to claim 50, wherein the differential high-gain device comprises
214 CMOS circuitry.

215
216 52. A circuit according to claim 48, further comprising the energy storage device.
217
218 53. A circuit according to claim 49, wherein the energy storage device comprises a
219 capacitor.
220
221 54. A circuit according to claim 50, wherein the energy storage device comprises a
222 double layer capacitor.
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224 55. A circuit according to claim 50, wherein the energy storage device comprises at least
225 two capacitors and a voltage balancer.
226
227 56. A circuit according to claim 48, wherein the differential high-gain device comprises
228 an operational amplifier.
229
230 57. A circuit according to claim 48, wherein the differential high-gain device comprises
231 CMOS circuitry.
232
233 58. A circuit according to claim 48, wherein the differential high-gain device comprises a
234 comparator.
235
236 59. A circuit according to claim 48, wherein the switch comprises a discrete transistor.
237
238 60. A circuit according to claim 48, wherein the switch comprises a discrete power
239 transistor.
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241 61. A circuit according to claim 48, wherein the switch comprises a MOSFET.
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243 62. A circuit according to claim 48, wherein the switch comprises an analog
244 semiconductor switch.
245

246 63. A method for coupling an energy storage device to an output of a power supply, the
247 method comprising:
248 coupling the energy storage device in series with a switch controllable by a switching
249 signal;
250 generating a feedback signal representing current flowing into the energy storage
251 device;
252 comparing the feedback signal to a predetermined control signal; and
253 generating the switching signal to turn off the switch when the comparing step
254 indicates that the current is not lower than a predetermined level.
255
256 64. A method for coupling an energy storage device to an output of a power supply, the
257 method comprising:
258 coupling the energy storage device in series with a switch controllable by a switching
259 signal;
260 generating a reference signal;
261 generating a signal representing voltage at the output of the power supply;
262 comparing the reference signal to the signal representing voltage at the output of the
263 power supply; and
264 generating the switching signal to turn off the switch when the comparing step
265 indicates that the voltage at the output of the power supply is below a predetermined
266 level.
267
268 65. A system for use with a power supply, comprising:
269 a load, the load coupled to output terminals of the power supply;
270 a charge storage device;
271 a current control device, the charge storage device and the current control device
272 coupled to output terminals of the power supply, wherein the current control device
273 controls current flowing through the charge storage device.
274
275 66. The system of claim 65, wherein the charge storage device comprises a capacitor.
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277 67. The system of claim 66, wherein the capacitor comprises a nominal operating voltage
278 of no more than about 3 volts.
279

280 68. The system of claim 66, wherein the capacitor comprises a double layer capacitor.
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282 69. The system of claim 66, wherein the capacitor comprises a value between 1 Farad and
283 5000 Farad.
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285 70. The system of claim 65, wherein the charge storage device comprises 2 series
286 connected capacitors, and wherein to the two series connected capacitors are coupled to a
287 voltage balancing circuit.
288

289 71. A circuit for use with a power supply, comprising:
290 a charge storage device device; and
291 a current control device, the charge storage device and the current control device
292 coupled to provide output terminals, wherein the current control device controls current
293 flowing through the charge storage device when the output terminals are coupled to the
294 power supply.
295

296 72. A circuit for use with a power supply, comprising:
297 charge storage means for storing charge; and
298 current control means for controlling current through the charge storage means when
299 the charge storage means and current control means are coupled to the power supply.
300
301